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PATENT & TRADEMARK OFFICE

NP012 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: David Meltzer, et al. Group Art Unit: Not Yet Assigned

Serial No.: 10/796,331 Examiner: Not Yet Assigned

Filed: March 8, 2004

Title: A Frequency/Phase Locked Loop Clock Synthesizer Using An All Digital Frequency Detector and An Analog Phase Detector

CERTIFICATE OF MAILING

I hereby certify that this Information Disclosure Statement and the documents attached hereto, are being deposited with the United States Postal Service with sufficient postage as First Class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date: March 23, 2004

Mary Bastida

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In compliance with the duty of disclosure under 37 C.F.R. §1.56, and in accordance with the practice under 37 C.F.R. §1.97 and §1.98, the Examiner's attention is directed to the document(s) listed on the enclosed Form PTO-1449. A copy of each listed document is enclosed, except, in the case where this application is filed after June 30, 2003, copies of any U.S. patents and U.S. patent application publications are not enclosed.

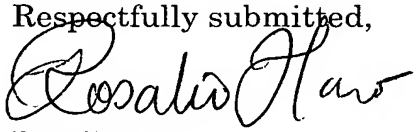
This Information Disclosure Statement is being filed within three months of the U.S. filing date or before the mailing date of a first Office Action on the merits. No statement or fee is required (37 CFR §1.97(b)).

CONCLUSION

The Commissioner is hereby authorized to charge any additional fees, which may be required, or credit any over-payment to Deposit Account No.: 19-2746.

It is respectfully requested that the above information be considered by the Examiner and that a copy of the enclosed Form PTO-1449 be initialed and returned indicating that such information has been considered.

Respectfully submitted,



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Form PTO-1449 | DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

SERIAL NO. 10/796,331	ATTY DOCKET NO. NP012
APPLICANT David Meltzer, et al.	
FILING DATE March 8, 2004	GROUP

INFORMATION DISCLOSURE CITATION
(USE SEVERAL SHEETS IF NECESSARY)
PAGE 1 OF 1

U.S. PATENT DOCUMENTS

E.I.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

FOREIGN PATENT DOCUMENTS

E.I.		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
	AL						
	AM						
	AN						
	AO						

OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

	AP	**F.M. Gardner, "Properties of Frequency Difference Detectors" IEEE Transactions on Communications Vol. COM –33, No. 2, February 1985, pp 131-138**
	AQ	**B. Razavi, "Design of Monolithic Phase-Locked Loops and Clock Recovery Circuits – A Tutorial" in Monolithic Phase-Locked Loops and Clock Recovery Circuits, Edited by Behzad Razavi, New York, IEEE Press, 1996**
	AR	**I. Hwang, S. Song, S. Kim, "A Digitally Controlled Phase-Locked Loop With a Digital Phase-Frequency Detector for Fast Acquisition", IEEE Journal of Solid-State Circuits, Vol. 36, No. 10, October 2001, PP 1574-1581**
	AS	**A. Hajimiri and T.H. Lee, "Design Issues in CMOS Differential LC Oscillators", IEEE Journal Of Solid-State Circuits, Vol. 34, No. 5, May 1999, pp 717-724**

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.